Motorola PowerPC™ Microprocessor Strategy

Core-Based Design
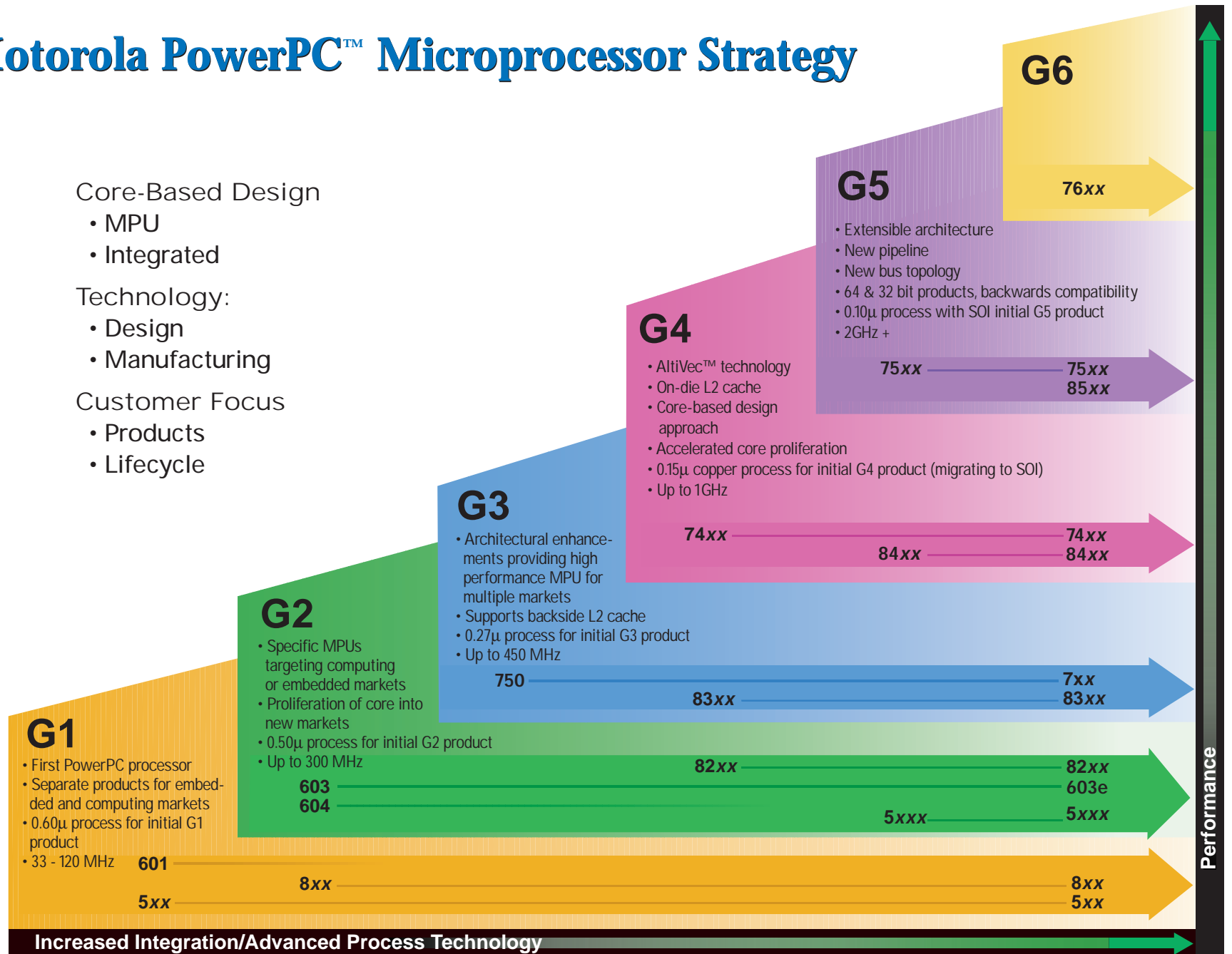- MPU
- Integrated

Technology:
- Design
- Manufacturing

Customer Focus
- Products
- Lifecycle

G6

76*xx*

G5
- Extensible architecture
- New pipeline
- New bus topology
- 64 & 32 bit products, backwards compatibility
- 0.10μ process with SOI initial G5 product
- 2GHz +

75*xx* ——— 75*xx*
85*xx*

G4
- AltiVec™ technology
- On-die L2 cache
- Core-based design approach
- Accelerated core proliferation
- 0.15μ copper process for initial G4 product (migrating to SOI)
- Up to 1GHz

74*xx* ——— 74*xx*
84*xx* ——— 84*xx*

G3
- Architectural enhancements providing high performance MPU for multiple markets
- Supports backside L2 cache
- 0.27μ process for initial G3 product
- Up to 450 MHz

750 ——— 7*xx*
83*xx* ——— 83*xx*

G2
- Specific MPUs targeting computing or embedded markets
- Proliferation of core into new markets
- 0.50μ process for initial G2 product
- Up to 300 MHz

82*xx* ——— 82*xx*
603 ——— 603e
604
5*xxx* ——— 5*xxx*

G1
- First PowerPC processor
- Separate products for embedded and computing markets
- 0.60μ process for initial G1 product
- 33 - 120 MHz

601 ———
8*xx* ——— 8*xx*
5*xx* ——— 5*xx*

Performance

Increased Integration/Advanced Process Technology

1991

200x

6xx, 7xx, 7xxx — high performance microprocessor targeting computing and high-end embedded
8xx, 8xxx — integrated processor targeting the Communications and Consumer markets
5xx, 5xxx — integrated processor targeting the Transportation market

9/99